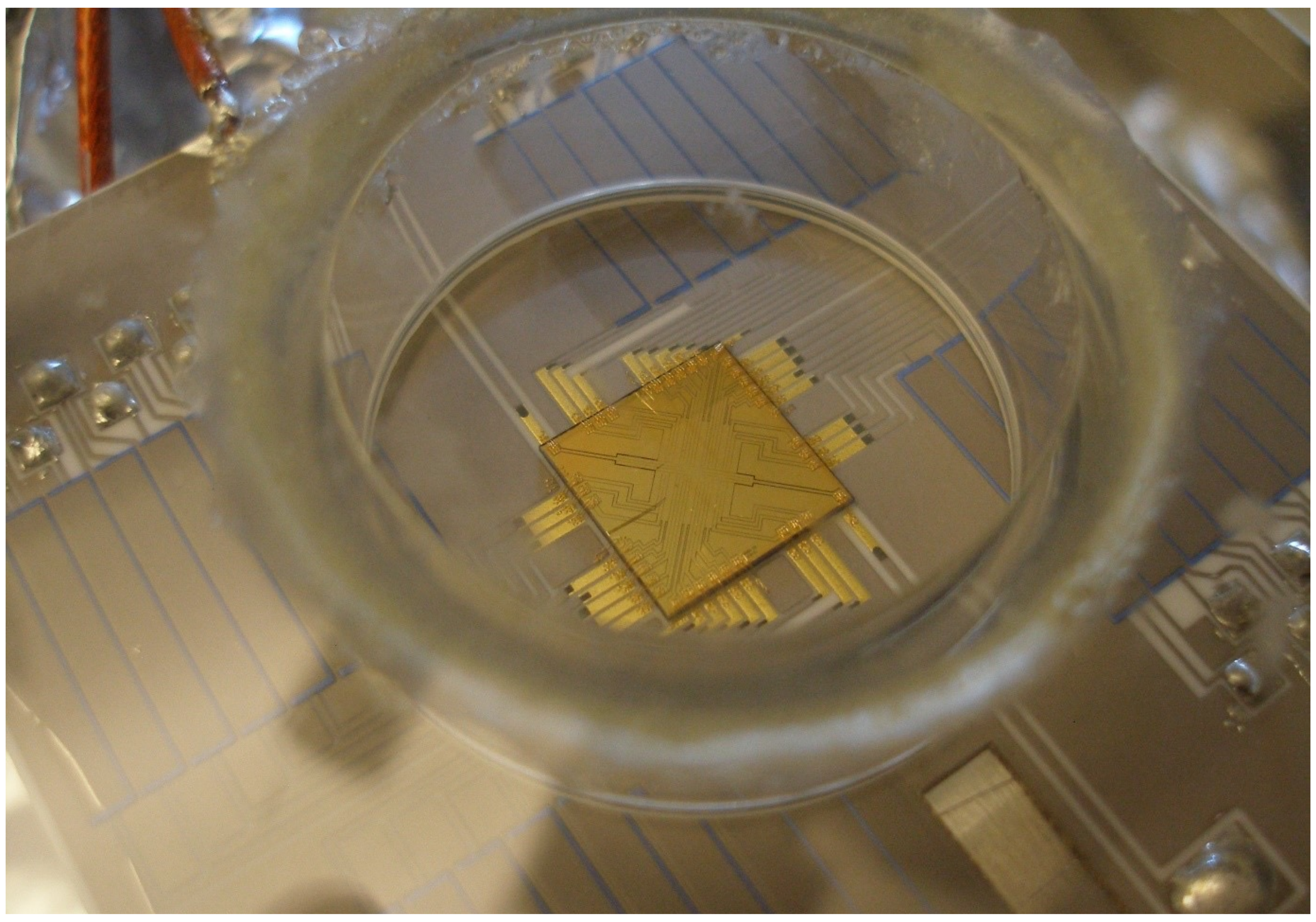
QSea II

QSea II is a project by NXP Semiconductors, eleQtron and ParityQC, commissioned by the DLR Quantum Computing Initiative (DLR QCI). The project's goal is to build modular and scalable ion-trap quantum computers, based on a universal quantum computer architecture. Each module will have its own small quantum processor with 10 qubits each, and the structure will have the potential to grow to comprise many chips with up to thousands of qubits.

- Ion traps
- Quantum Computer



Objective

The goal of QSea II is to develop a modular and scalable advancement of the QSea I demonstrator. The QSea II quantum computer will be based on a MAGIC quantum processor, developed by eleQtron, coupled with ParityQC's quantum architecture. MAGIC stands for Magnetic Gradient Induced Coupling: it is a technology developed by eleQtron that enables the precise control of qubits using inexpensive and miniaturizable high-frequency technology.

ParityQC is in charge of the development of a high-performing compiler, operating system, efficient error correction as well as hardware-specific algorithms for the quantum device. The team is also developing the digital twin of the quantum computer, to speed up the design and optimized performance of the device.

Finally, NXP Semiconductors is contributing its valuable expertise in industrial projects and innovative industrial applications. NXP will make use of its know-how in systems electronics for the scaling and miniaturization of components and for the chip-based photon detection for reading out quantum states.

Motivation

The overarching goal of the consortium is to make innovations in quantum technologies socially usable and to transfer them to commercial applications.

Quantum computers based on trapped ions are considered extremely strong candidates in the race toward practical and scalable quantum computing. The advantages of ion-trap systems lie in their stability, precision, and scalability potential.

Within QSea II, the project members aim to develop a modular and scalable full-stack system, with unique technical features both from the hardware and from the software side. It will enable the DLR and its partners to immediately work with the novel machine once it is delivered at the completion of the project.

The modular and scalable approach is essential in the QSea II project, and it is an answer to the key challenges currently existing in the quantum computing industry. Scalability is a challenge because it is difficult to increase the number of qubits in a device while maintaining low error rates, qubit coherence, and reliable control. Modular and scalable chips can help address the scalability challenge in quantum computing. By creating smaller modules of chips that can be interconnected, these systems can reduce the complexity of managing large numbers of qubits in a single device. Modular architectures allow for easier scaling by linking multiple smaller, well-controlled quantum processors (in this case, based on the MAGIC method), enabling large-scale quantum computation.

Innovation

Our modular, scalable quantum computer is based on novel surface trap chips being developed by eleQtron. Basic functionalities for controlling and detecting the qubits are integrated into these ion-trap chips, each of which is already a single fully functional quantum processor. Several such sub-processors are connected either by optically coupling the qubits or by transporting the ions from one microchip to another. The ParityQC Architecture allows algorithms to be efficiently developed on these modular chips to solve real-world problems in a wide range of application areas. Whereas NXP focuses on adapting the system and detection electronics to cryogenic environments.

Timeline and main activities

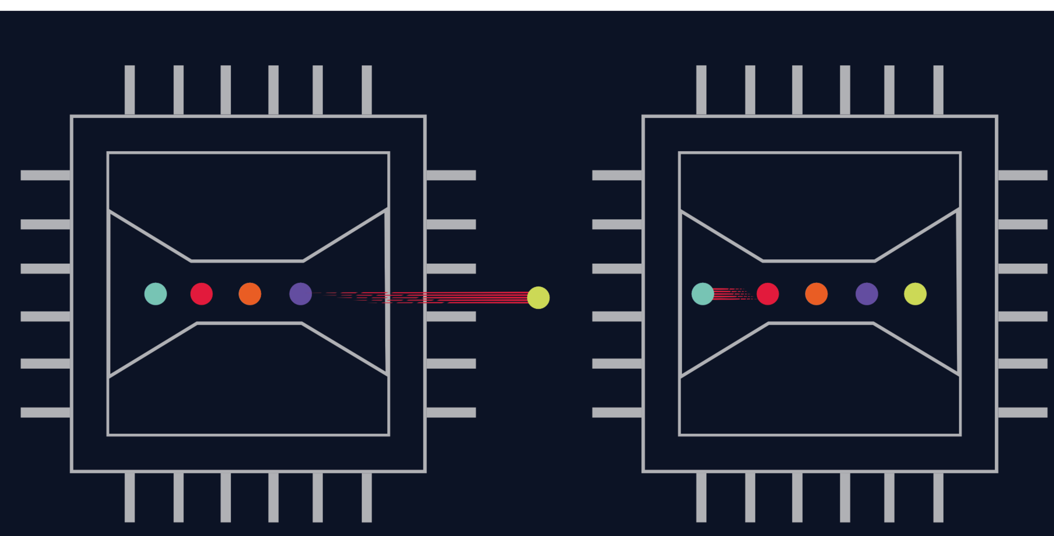
In November 2024, the lab space at the DLR QCI Innovation center has been provided, in order to start the set up of the QSea II quantum computer.

In this phase, the primary focus will be the installation and test of the initial prototype of the quantum chips that will be used for the modular structure of the device. Inside these chips, all qubits are coupled to one another using magnetic field gradients, based on the MAGIC method.

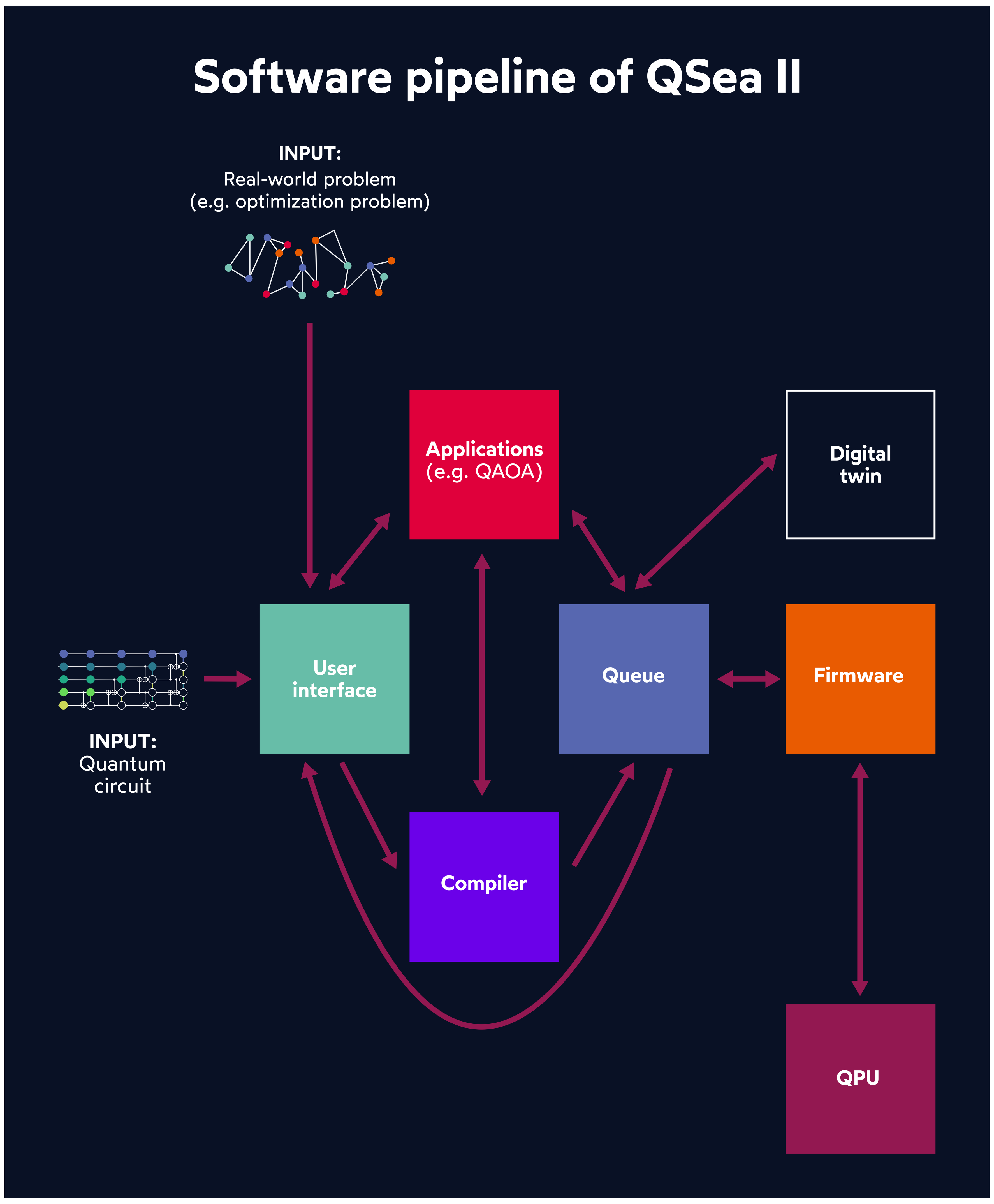
NXP develops SPADs (Single-Photon Avalanche Diodes) and control chips for ion-trap quantum computers to enable high-precision photon detection and fast, reliable control of quantum states. These components are crucial for managing the delicate interactions within ion traps, allowing for precise quantum state manipulation and data readout essential to quantum computing. By advancing SPAD and control chip technology, NXP contributes to the scalability and efficiency needed to make ion-trap quantum computers like QSea II commercially viable.

In addition to contributing the innovative features of the ParityQC Architecture to achieve a modular and scalable structure of the quantum chips, ParityQC will also focus on the software side. The team will develop a digital twin for the quantum device (suitable for a modular setup) and a hardware-specific compiler. A co-design algorithm for solving optimization problems will also be developed, and it will be optimized for modular quantum computing. The goal is to develop a highly efficient operating system which will be easy to operate, without the need for the user to be highly proficient in quantum algorithms.

The QSea II project will end in February 2027, with the official delivery of the quantum computer to DLR QCI.



Two ion trap modules connected by ion shuttling



More information about the project on the websites of DLR QCI and QSea

qci.dlr.de/en/qsea-ii *q-sea.de*

A project of

Contractors

Contact

Till Witt, Project Manager, **NXP Semiconductors** / till.witt@nxp.com

Christian Piltz, Senior Quantum Engineer and Site Lead, **eleQtron** / christian.piltz@eleqtron.com

Christian Ertler, Co-Head of Technology Partnerships, **ParityQC** / c.ertler@parityqc.com

Get in touch.
We enable quantum!

Supported by:

Federal Ministry for Economic Affairs and Climate Action

on the basis of a decision by the German Bundestag